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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/017,855 | 12/14/2001 | Philip A. Fisher | 039153-0441 (GO406) | 9701 |

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| EXAMINER | |
|---|---|
| MALDONADO, JULIO J | |
| ART UNIT | PAPER NUMBER |
| 2823 | |

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/017,855 | FISHER ET AL. | |
| | Examiner | Art Unit | |
| | Julio J. Maldonado | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 and 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

1. Applicant's cancellation to claims 15-20 is acknowledged. Claims 21-26 are newly added. Thus, claims 1-14 and 21-26 are pending in this application.

### *Election/Restrictions*

2. Applicant's election with traverse of claims 1-14 in Paper No. 6 is acknowledged. The traversal is on the ground(s) that non-elected claims 15-20 were cancelled.

### *Claim Objections*

3. Claim 1 is objected to because of the following informalities: in reference to claim 1, where applicants recite "...transferring the trimmed transistor gate pattern to a layer disposed below the photoresist layer..." should recite "...transferring the trimmed transistor gate pattern to a layer disposed below said trimmed pattern...". Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-14 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auda et al. (U.S. 5,139,904) in view of Tsai et al. (U.S. 6,183,937 B1).

In reference to claims 1, 4, 7, 8, 11 and 21, Auda et al. (Figs.2A-2D) in a related patterning process teach patterning a transistor gate pattern (17a) on a photoresist layer (17); curing the transistor gate pattern (17a); trimming the cured transistor gate pattern

(17a); and transferring the trimmed transistor gate pattern (17a') to a layer (16) disposed below said trimmed pattern (17a') to form a transistor gate (16a) (column 5, line 30 – column 6, line 17).

However, Auda et al. fail to teach curing the transistor gate pattern with an electron beam, wherein the transistor gate pattern includes a width and a length, and a variation of the width along the length of the transistor gate is reduced due to the curing step. However, Tsai et al. (Figs.5-9) in a related method to pattern a transistor gate teach depositing a photoresist layer (38) on a layer (38) used to form the gate electrode; patterning a transistor gate pattern (38a) on a photoresist layer (38); curing the transistor gate pattern (38a) with an electron beam, wherein the transistor gate pattern includes a width and a length, and a variation of the width along the length of the transistor gate is reduced due to the curing step (column 8, line 6 – column 11, line 46). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to cure the gate pattern as taught by Tsai et al. in the patterning process of Auda et al., since this cure process decompose a conformal surface layer of the patterned photoresist layer while simultaneously forming a patterned photoresist layer having a second linewidth narrower than the first linewidth (column 3, lines 44 – 49).

The combined teachings of Auda et al. and Tsai et al. substantially teach all aspects of the invention but fail to show wherein the final gate transistor width is in the range of approximately 20-60 nm, and wherein the uniformity of the gate width is 4 to 6 nm over 3 nm segment. Notwithstanding, it would have been an obvious matter of

design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claims 2, 3, 14, 25 and 26, the combined teachings of Auda et al. and Tsai et al. teach wherein the photoresist layer is comprised of a photoresist material used for of 248 lithography and is commercially available (Tsai et al., column 6, lines 26 – 46).

In reference to claims 5, 6, 9, 10 and 22, the combined teachings of Auda et al. and Tsai et al. substantially teach all aspects of the invention but fail to expressly teach wherein the curing step includes exposing the transistor gate pattern to the electron beam having a dose in the range of approximately 100-100,000 $\mu C/cm^2$; and wherein the curing step includes exposing the transistor gate pattern to the electron beam having an accelerating voltage in the range of approximately 5-50,000 Volts. However,

since the operating parameters of the curing step are performed in the same wavelength obtaining the same result (reduction in linewidth), it would have been obvious to one of ordinary skill in the art at the time the invention was made that the electron beam would have a dose in the range of approximately 100-100,000 $\mu C/cm^2$ and an accelerating voltage in the range of approximately 50-2,000 Volts.

In reference to claims 7, 13 and 24, the combined teachings of Auda et al. and Tsai et al. teach wherein the curing step includes changing at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the transistor gate (column 8, line 6 – column 11, line 46).

In reference to claims 12 and 23, the combined teachings of Auda et al. and Tsai et al. teach wherein the photoresist layer is comprises of a material selected from a group consisting of a phenolic-based polymer (Tsai et al., column 2, lines 29 – 65).

***Conclusion***

6. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-

mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
6/13/03

George Fourson
Primary Examiner